# EXHIBIT 8

*Williams Wireless Technologies et al.*
*v.*
*Research in Motion, et al.*

# Plaintiffs' Amended Disclosures Pursuant to Local Rule 3-1

## Infringing Instrumentalities of:

## Kyocera Mita America, Inc.

# STATEMENT REGARDING ACCUSED

# KYOCERA'S WIRELESS COMMUNICATIONS PRODUCTS

The accompanying claim charts explain the basis for infringement of claims 1, 2, 3, 4, 6 and 7 of U.S. Patent No. 4,809,297 (the '297 Patent) by Kyocera's wireless communications products. Various versions of Kyocera's products incorporate wireless communication devices that interface with the conventional cellular telephone system, including various CDMA based telecommunications networks. Accordingly, the Kyocera's products necessarily incorporate CDMA wireless chipsets that are compatible with the the CDMA cellular networks. Accordingly, Kyocera's products incorporate one or more of the chipsets identified below in the following claim charts, which are chipsets designed to communicate with CDMA cellular networks.

These bases apply to all of Kyocera's presently identified products including the wireless mobile phones identified in the Complaint and hereinafter, which, for purposes of this action, are believed to be functionally equivalent from an infringement standpoint.

Williams Wireless Technologies and Polansky Electronics, Ltd. reserve the right to refine and improve the claim charts as discovery progresses and, in particular, after Kyocera provides full information regarding its products pursuant to Local Rule 3-4. In addition, Williams Wireless Technologies and Polansky Electronics, Ltd reserve the right to supplement the claim charts once they are provided with discovery regarding each of the Kyocera wireless communications devices named herein and have had an opportunity to obtain testimony on the accused and suspected products from Kyocera.

Unless otherwise stated herein, the specified element of each asserted claim is believed to be literally present in the accused instrumentality.

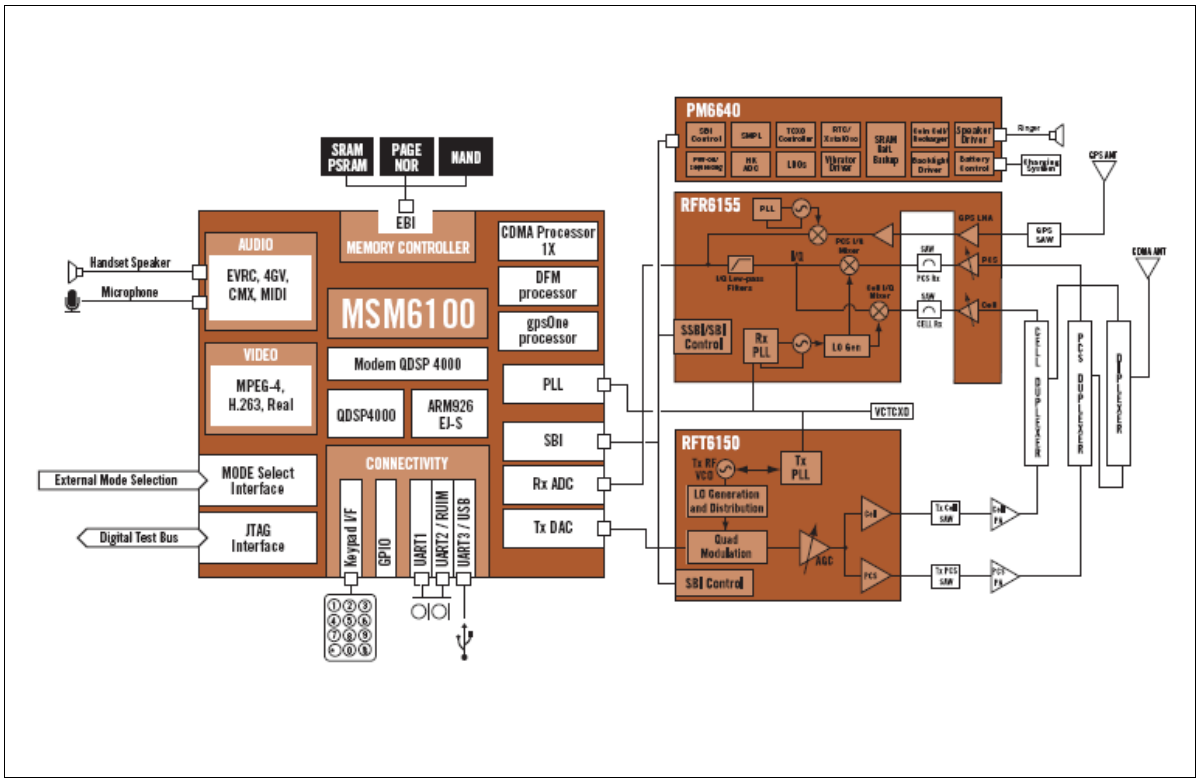
Pursuant to Local Rule 3-1, and for each claim asserted hereinafter, Williams Wireless Technologies and Polansky Electronics, Ltd. identify the following:

Williams Electronics Limited F.M.I.D. Facsimile Mobile Interface Data Device Model R100-5767.

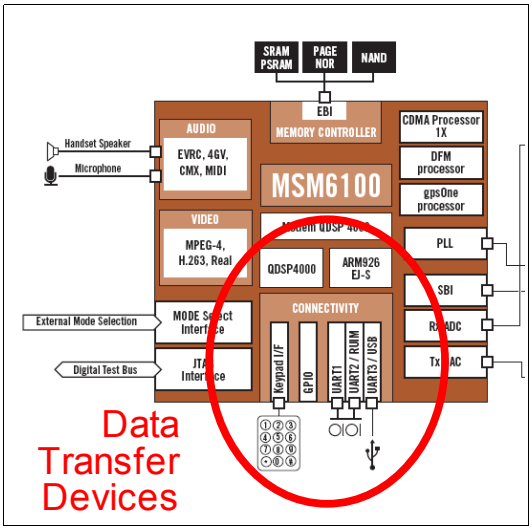
## MSM6100 Chipset

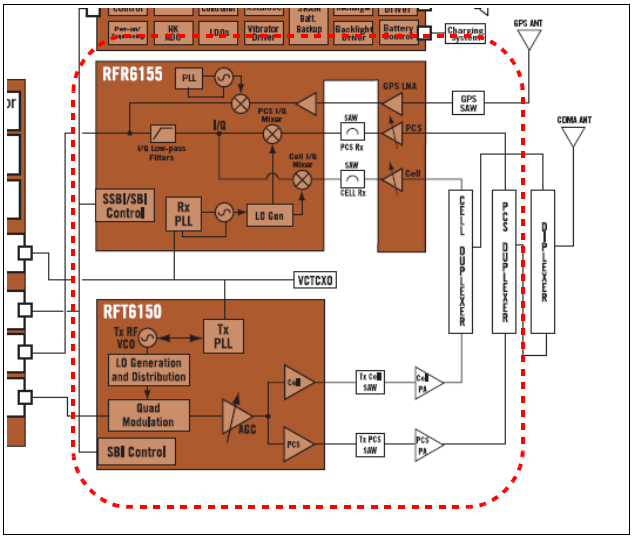
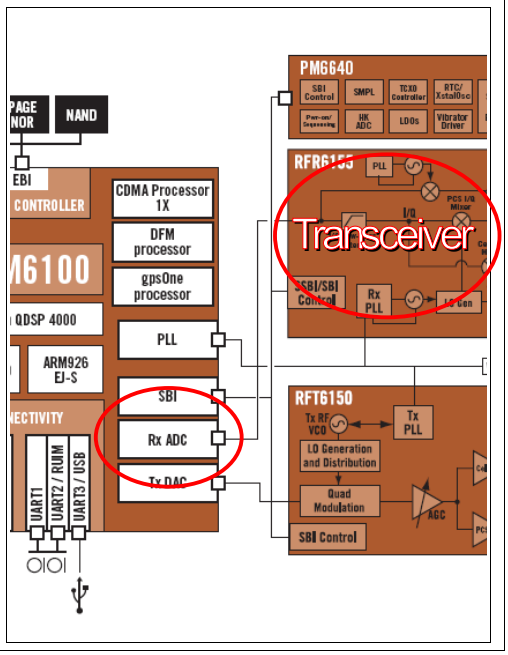
Certain of Kyocera's wireless mobile devices, in particular at least the KX2/Koi, have been manufactured and delivered incorporating the Qualcomm® MSM6100 chipset solution (pictured below). The MSM6100 chipset includes circuitry and componentry that causes the device to interface a data transfer device with a radio transceiver, as claimed in U.S. Patent 4,809,297.

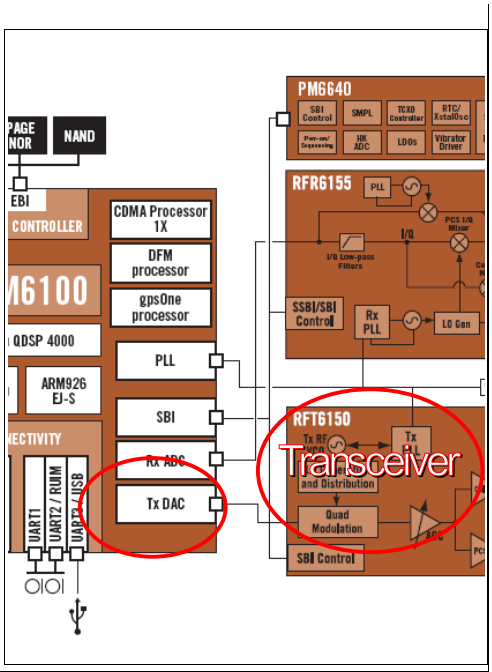
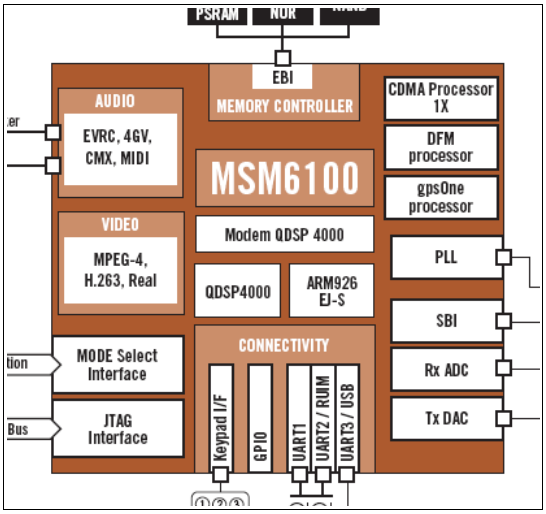
Plaintiff further alleges that other devices manufactured by Kyocera and other Defendants that incorporate the identified chipset also infringe in the same manner as detailed below. For the purpose of this Claim Chart, an "accused instrumentality" is any device of the Defendant that incorporates the MSM6100 chipset.

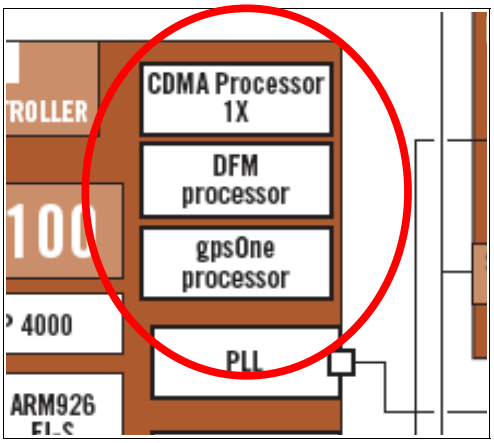


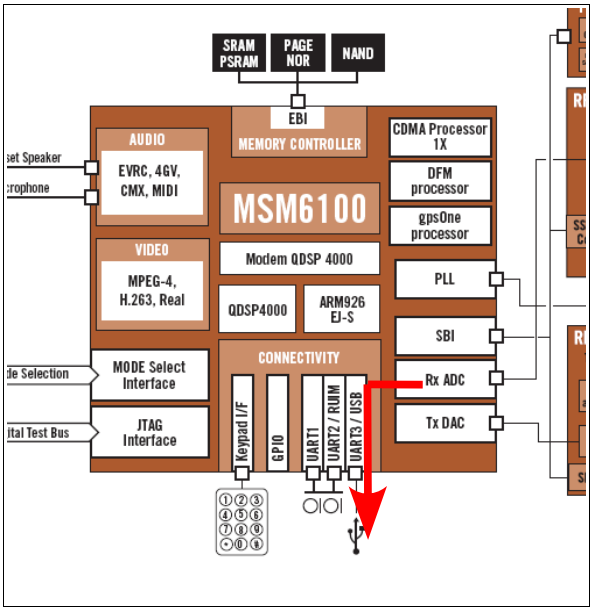
# CLAIM CHART

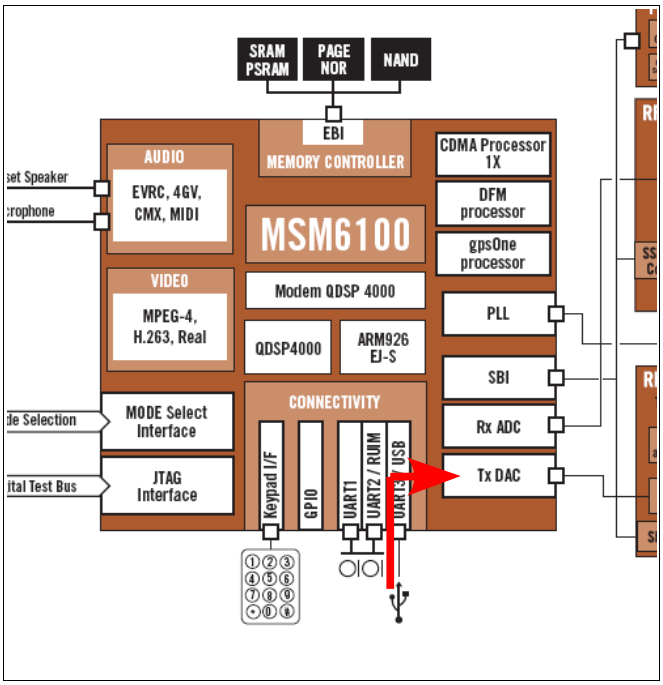
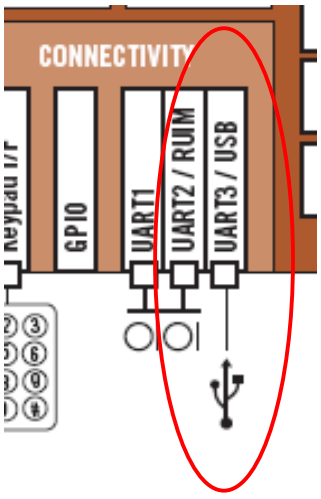
| | |
|---|---|
| 1. An interface to connect a data transfer device with a radio transceiver<br><br>*comprising:* | The accused device includes the chipset identified above, which is an interface to connect a data transfer device with a radio transceiver.<br><br>The accused device includes several components, any one or more of which constitute a data transfer device. In one example, the accused device includes at least a keyboard, which is a data transfer device.<br><br>Other components coupled to the identified chipset may also constitute a "data transfer device", such as any one or more devices connected to the "Connectivity" portion of the identified chipset below.<br><br>  <br> |
| | The accused device further includes a radio transceiver as identified in the representative chipset diagram reproduced below. The components constituting the radio transceiver include the RFR6155, and RFT6150 components. |

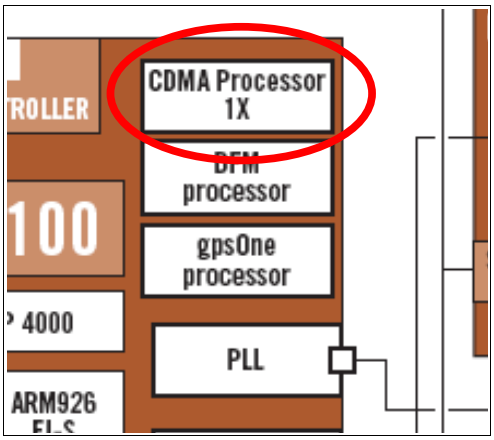
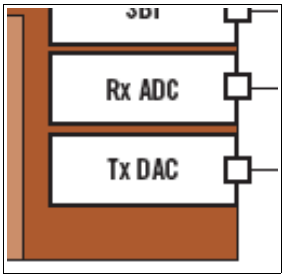
| | |
|---|---|
| |  <br>Transceiver Portion of MSM6100 Chipset |
| a **receiving circuit** to receive a data signal in a given form from said **transceiver**, | The identified chipset embedded in the accused instrumentality includes a receiving circuit shown here as the "RX ADC" (receiving analog-to-digital converter).<br><br>The receiving circuit receives a data signal in a given form from the transceiver, identified here as component RFR6155.  |

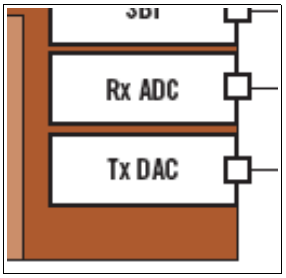
| | |
|---|---|
| a **transmitting circuit** to transmit a data signal in said given form to said **transceiver**, | The identified chipset embedded in the accused instrumentality includes a receiving circuit shown here as the "TX DAC" (transmitting digital-to-analog converter).<br><br>The transmitting circuit transmits a data signal in a given form to the transceiver, identified here as component RFT6150.<br><br>  |
| a data bus to transfer one of said data signals between said device and the respective circuit, | The identified chipset component includes a data bus within the MSM6100 chip that operates to transfer data between the data transfer device and the receiving circuit, and to transfer data between the data transfer device and the transmitting circuit.<br><br>In the accused instrumentalities, the data bus is at least partially contained within the integrated circuit forming the MSM6100 chip as a series of etched conductive paths or links between the functional blocks illustrated below in the chip set. The data bus also further includes or couples to any of the dual memory buses, the general-purpose interface bus, the address/data microprocessor bus and other internal buses<br><br>  |

| | |
|---|---|
| switch means to connect one of said circuits with said data bus | The accused instrumentalities include switch means that connect one of the receiving or transmitting circuits with the data bus. The identified chipset includes transistors and other logic gates for alternately coupling components of the chipset one to another for the purpose of isolating, blocking, routing and or conditioning of the data signals to connect the data bus with either of the receiving or transmitting circuits.<br><br>The switch means comprises various logic gates and transistors that are in electrical cooperation with each of the various sub-components of the identified chip set that perform the function of the switch means. These various logic gates and transistors function to effectively connect the transmitting circuit or the receiving circuit to the data bus. |
| and control means to control said switch means, | The accused instrumentalities include electronic circuitry operable to control the switch means, to connect one of the transmitting or receiving circuits with the data bus.<br><br>The control means is a microprocessor or digital signal processor (DSP) in the accused instrumentality executing code that provides logic for determining whether to connect one of the transmitting or receiving circuits with the data bus. The microprocessor is under control of the source code is a special purpose machine including various logic gates and transistors, such as AND gates, flip-flops and inverters, that perform the function of the control means. Such control means along with the switch means described above can be found in the CDMA processor, the gpsOne processor, and the DFM processor portions of the chipset illustrated below.<br><br>  <br><br>These processors control the switching means to effectively connect the transmitting circuit of the receiving circuit to the data |

| | |
|---|---|
| | bus, to control the operation of the bus connection according to the intended destination of the signal to of from the data transfer device, to follow the change in the operational mode, to disconnect the connection in the unwanted route, and to maintain the effective connection in the wanted route. |
| said control means being responsive to a signal from said data transfer device, | In the accused instrumentalities, the control means responds to a signal from any one or more of the data transfer devices. The signal comprises a change of state in one or more data bits that signals a change in the operational mode of the data transfer device and/or data ready to be transmitted or otherwise handled by the control means on behalf of the data transfer devices. |
| which is indicative of a change in the operational mode thereof | In the accused instrumentalities, the signal from the data transfer device consists of one or more bi-stable digital bits having states of logic "1" and logic "0" indicative of a change in operational mode respectively. A change from logic "0" to logic "1" or vice versa indicates a change in the operational mode of the data transfer device. |
| to disconnect said one circuit | In the accused instrumentalities, a change in logic state of the signal received from the data transfer device, results in the control means and switch means operatively terminating effective communication between one of the transmitting or receiving circuits over the data bus.   |

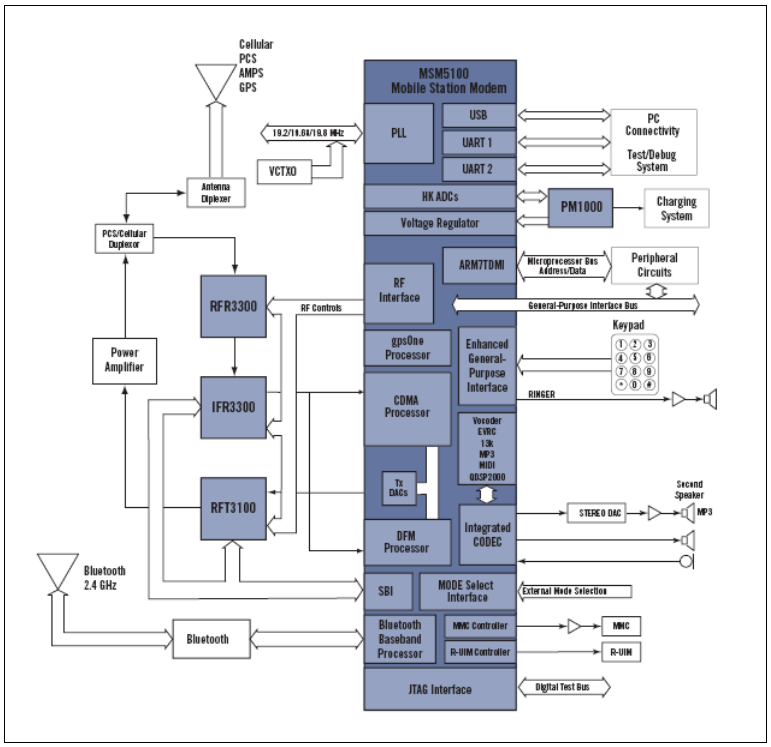
| | |
|---|---|
| and connect the other of said circuits to said data bus. | In the accused instrumentalities, a change in logic state of the signal received from the data transfer device, results in the control means and switch means operatively permitting effective communication between the other of the transmitting or receiving circuits over the data bus.<br>  |
| 2. An interface according to claim 1<br><br>wherein said signals are transferred between said data transfer device and said transceiver in serial form. | The accused instrumentalities include each of the elements specified by Claim 1.<br><br>In addition, the RX ADC and the TX DAC included in the chip sets used in each accused instrumentality each use a serial bus to transfer data with the transceiver. Accordingly, data are transferred between the data transfer device and the transceiver in serial form in the accused instrumentalities.<br><br>Moreover, in instances where the data transfer device is implemented as a component attached to the Universal Serial Bus (USB), the data signals are necessarily being transferred serially, which is an inherent feature of the Universal Serial Bus, illustrated at the right.<br>  |

| | |
|---|---|
| 3. An interface according to claim 2<br><br>wherein said control means operates upon said transceiver to condition said transceiver to a transmit mode upon connection of said databus with said transmitting circuit. | The accused instrumentalities include each of the elements specified by Claim 2.<br><br>In addition, the control means in the form of a microprocessor or digital signal processor, such as the CDMA processor illustrated below, executing code functions to direct the transceiver to transmit when the control means and switch means operate to enable communication of data from the transmitting circuit to the transceiver over the data bus.<br>  |
| 4. An interface according to claim 2<br><br>wherein said control means is responsive to a change from an inactive to an active condition to connect said data bus to said transmitting circuit. | The accused instrumentalities include each of the elements specified by Claim 2.<br><br>In addition, the control means in the form of a microprocessor executing code functions to enable data transfer from the data bus to the transmitting circuit when the user desires to communicate information. Such activation is indicated by a change in logic state in one or more logic bits within the microprocessor executing the code. |
| 6. An interface according to claim 4<br><br>including amplifying means in said receiving circuit. | The accused instrumentalities include each of the elements specified by Claim 4.<br><br>The RX ADC, illustrated to the right, includes amplifying circuitry.<br>  |

| | |
|---|---|
| 7. An interface according to claim 6<br><br>wherein a buffer amplifier is included in said transmitting circuit to isolate said switch means and said transceiver. | The accused instrumentalities include each of the elements specified by Claim 6.<br><br>In addition, the TX DAC, illustrated to the right, includes buffer amplifier circuitry that effectively isolates the switch means and the transceiver.<br><br>  |

**MSM5100 Chipset**

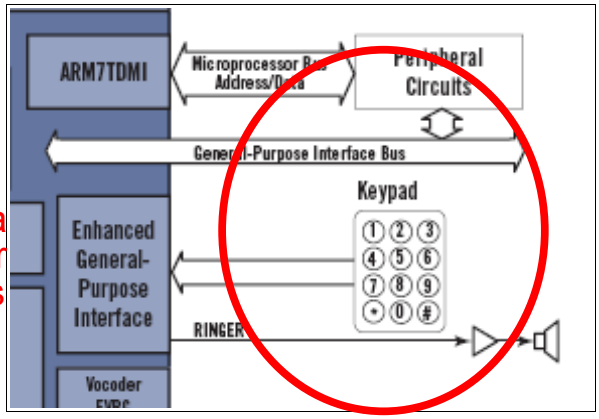
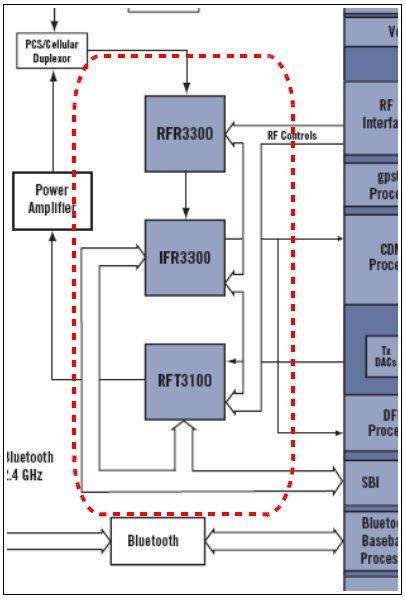
Certain of Kyocera's wireless mobile devices, in particular at least the KX444, have been manufactured and delivered incorporating the Qualcomm® MSM5100 chipset solution (pictured below). The MSM5100 chipset includes circuitry and componentry that causes the device to interface a data transfer device with a radio transceiver, as claimed in U.S. Patent 4,809,297.

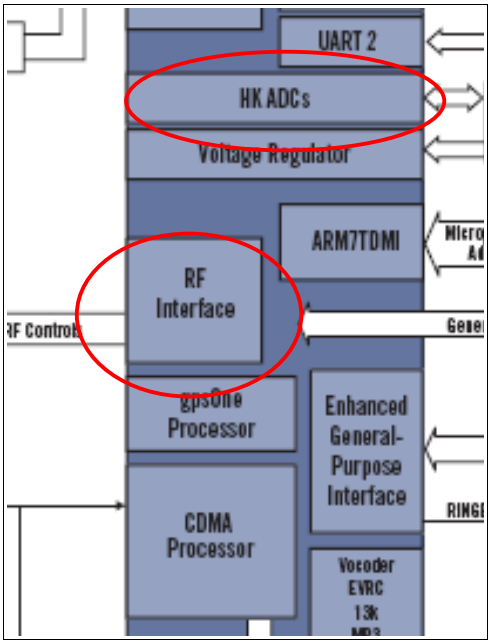
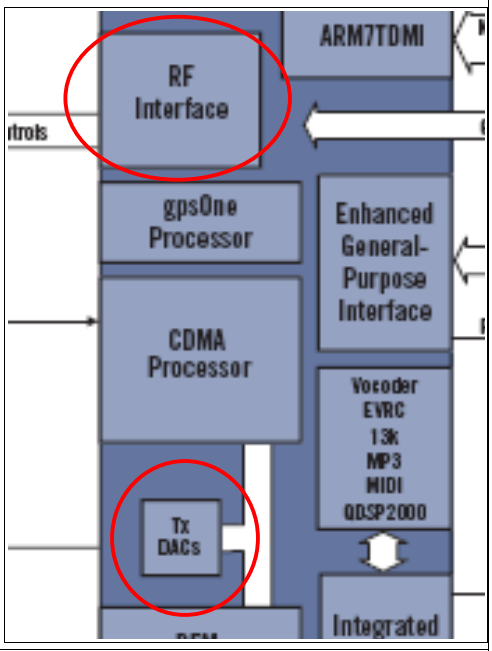


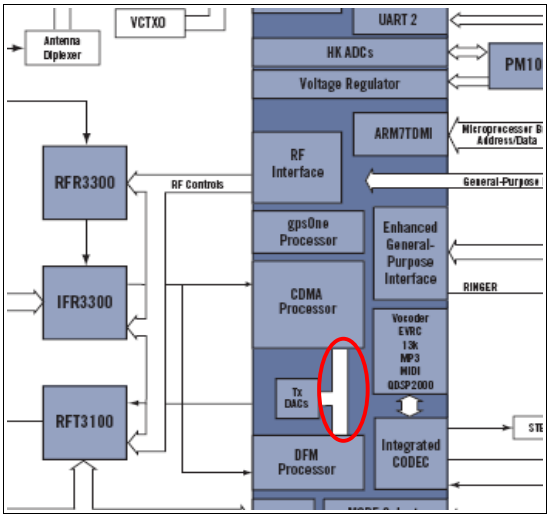
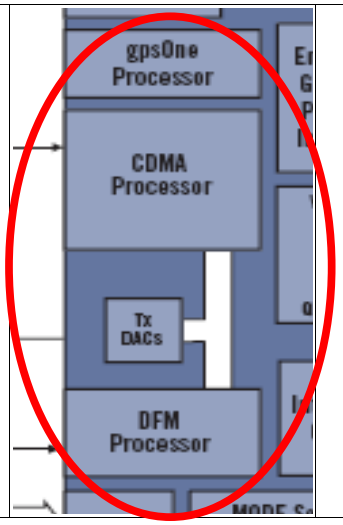

In particular, the OnStar syste device has been manufactured and delivered incorporating the Qualcomm® MSM5100 chipset solution (pictured at right). The MSM5100 chipset includes circuitry and componentry that causes the device to interface a data transfer device with a radio transceiver, as claimed in U.S. Patent 4,809,297.

Plaintiff further alleges that other devices manufactured by Kyocera and other Defendants that incorporate the identified chipset also infringe in substantially the same manner as detailed below.

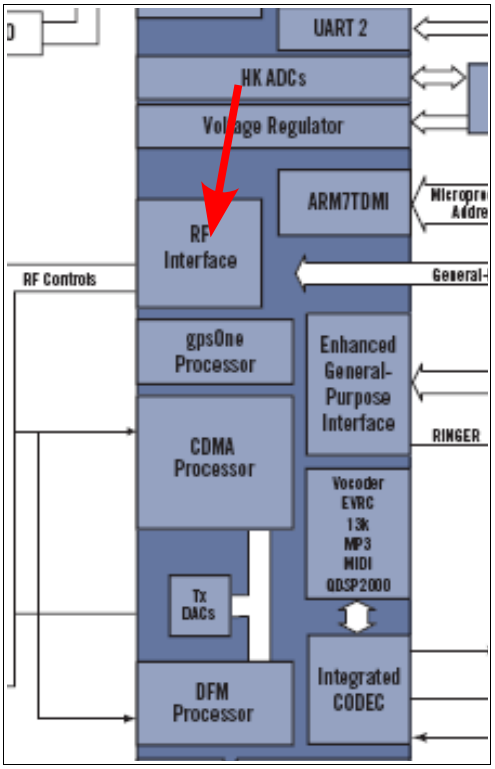
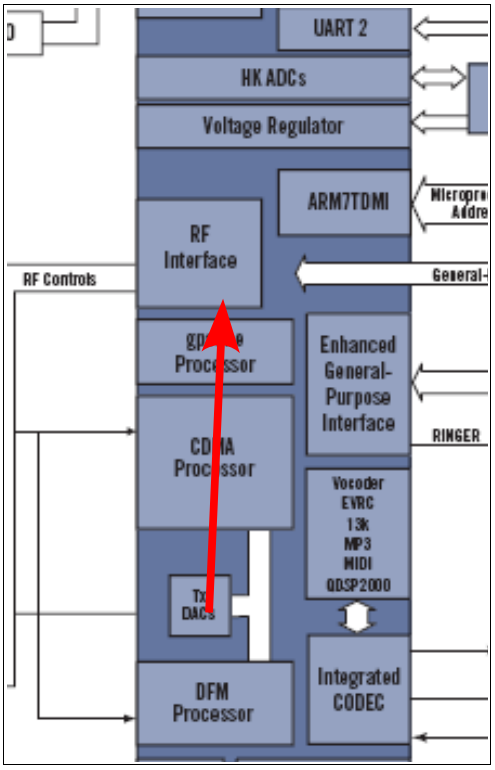
# CLAIM CHART

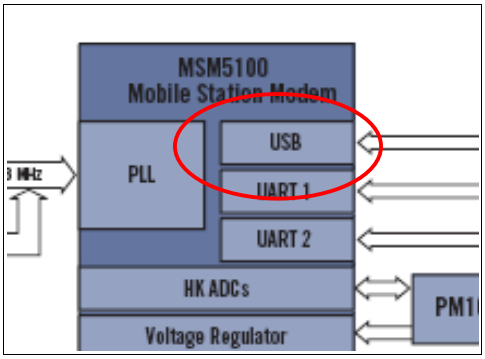
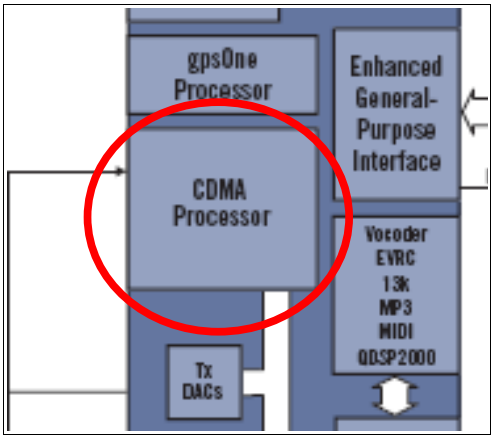
| | |
|---|---|
| 1. An interface to connect a data transfer device with a radio transceiver<br><br>*comprising:* | The accused device includes the chipset identified above, which is an interface to connect a data transfer device with a radio transceiver.<br><br>The accused device includes several components, any one or more of which constitute a data transfer device. In one example, the accused device includes a GPS receiver which is a data transfer device.<br><br>Other components coupled to the identified chipset may also constitute a "data transfer device", such as any one or more devices connected to the "Enhanced General-Purpose Interface" or the "General-Purpose Interface Bus" portions of the identified chipset, illustrated below.<br><br>Data Transfer Devices<br>  |
| | The accused device further includes a radio transceiver as identified in the representative chipset diagram reproduced at the right. The components constituting the radio transceiver include the RFR3300, and RFT3100 components, and their associated RF sub-components, such as the RF interface, antenna, filter, duplexer, etc.<br><br>Transceiver Portion of MSM5100 Chipset<br>  |

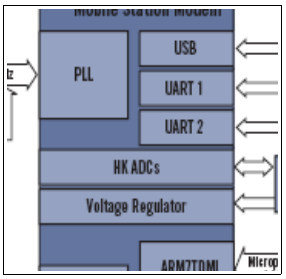
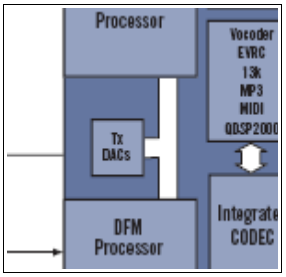
| | |
|---|---|
| a **receiving circuit** to receive a data signal in a given form from said **transceiver**, | The identified chipset embedded in the accused instrumentality includes a receiving circuit shown here as the "HK ADC" (receiving analog-to-digital converter).<br><br>The receiving circuit receives a data signal in a given form to the transceiver via the RF Interface component identified here.<br><br>  |
| a **transmitting circuit** to transmit a data signal in said given form to said **transceiver**, | The identified chipset embedded in the accused instrumentality includes a receiving circuit shown here as the "TX DAC" (transmitting digital-to-analog converter).<br><br>The transmitting circuit transmits a data signal in a given form to the transceiver via the RF interface component identified here.<br><br>  |
| a **data bus** to transfer one of said data signals between said device and the respective circuit, | The identified chipset component includes a data bus within the MSM5100 chip that operates to transfer data between the data transfer device and the receiving circuit, and to transfer data between the data transfer device and the transmitting circuit.<br><br>In the accused instrumentalities, the data bus is at least partially contained within the integrated circuit forming the MSM5100 chip as a series of etched conductive paths or links between the functional blocks illustrated below in the chip set. The data bus also further includes or couples to any of the dual memory buses, |

| | |
|---|---|
| | the general-purpose interface bus, the address/data microprocessor bus and other internal buses.<br>  |
| switch means to connect one of said circuits with said data bus | The accused instrumentalities include switch means that connect one of the receiving or transmitting circuits with the data bus. The identified chipset includes transistors and other logic gates for alternately coupling components of the chipset one to another for the purpose of isolating, blocking, routing and or conditioning of the data signals to connect the data bus with either of the receiving or transmitting circuits.<br><br>The switch means comprises various logic gates and transistors that are in electrical cooperation with each of the various sub-components of the identified chip set that perform the function of the switch means. These various logic gates and transistors function to effectively connect the transmitting circuit or the receiving circuit to the data bus. |
| and control means to control said switch means, | The accused instrumentalities include electronic circuitry operable to control the switch means, to connect one of the transmitting or receiving circuits with the data bus.<br><br>The control means is a microprocessor or digital signal processor (DSP) in the accused instrumentality executing code that provides logic for determining whether to connect one of the transmitting or receiving circuits<br>  |

| | |
|---|---|
| | with the data bus. The microprocessor is under control of the source code is a special purpose machine including various logic gates and transistors, such as AND gates, flip-flops and inverters, that perform the function of the control means. Such control means along with the switch means described above can be found in the CDMA processor, the gpsOne processor, and the DFM processor portions of the chipset illustrated here.<br><br>These processors control the switching means to effectively connect the transmitting circuit of the receiving circuit to the data bus, to control the operation of the bus connection according to the intended destination of the signal to of from the data transfer device, to follow the change in the operational mode, to disconnect the connection in the unwanted route, and to maintain the effective connection in the wanted route. |
| said control means being responsive to a signal from said data transfer device, | In the accused instrumentalities, the control means responds to a signal from any one or more of the data transfer devices. The signal comprises a change of state in one or more data bits that signals a change in the operational mode of the data transfer device and/or data ready to be transmitted or otherwise handled by the control means on behalf of the data transfer devices. |
| which is indicative of a change in the operational mode thereof | In the accused instrumentalities, the signal from the data transfer device consists of one or more bi-stable digital bits having states of logic “1” and logic “0” indicative of a change in operational mode respectively. A change from logic “0” to logic “1” or vice versa indicates a change in the operational mode of the data transfer device. |

| | | |
|---|---|---|
| to disconnect said one circuit | In the accused instrumentalities, a change in logic state of the signal received from the data transfer device, results in the control means and switch means operatively terminating effective communication between one of the transmitting or receiving circuits over the data bus. |  |
| and connect the other of said circuits to said data bus. | In the accused instrumentalities, a change in logic state of the signal received from the data transfer device, results in the control means and switch means operatively permitting effective communication between the other of the transmitting or receiving circuits over the data bus. |  |

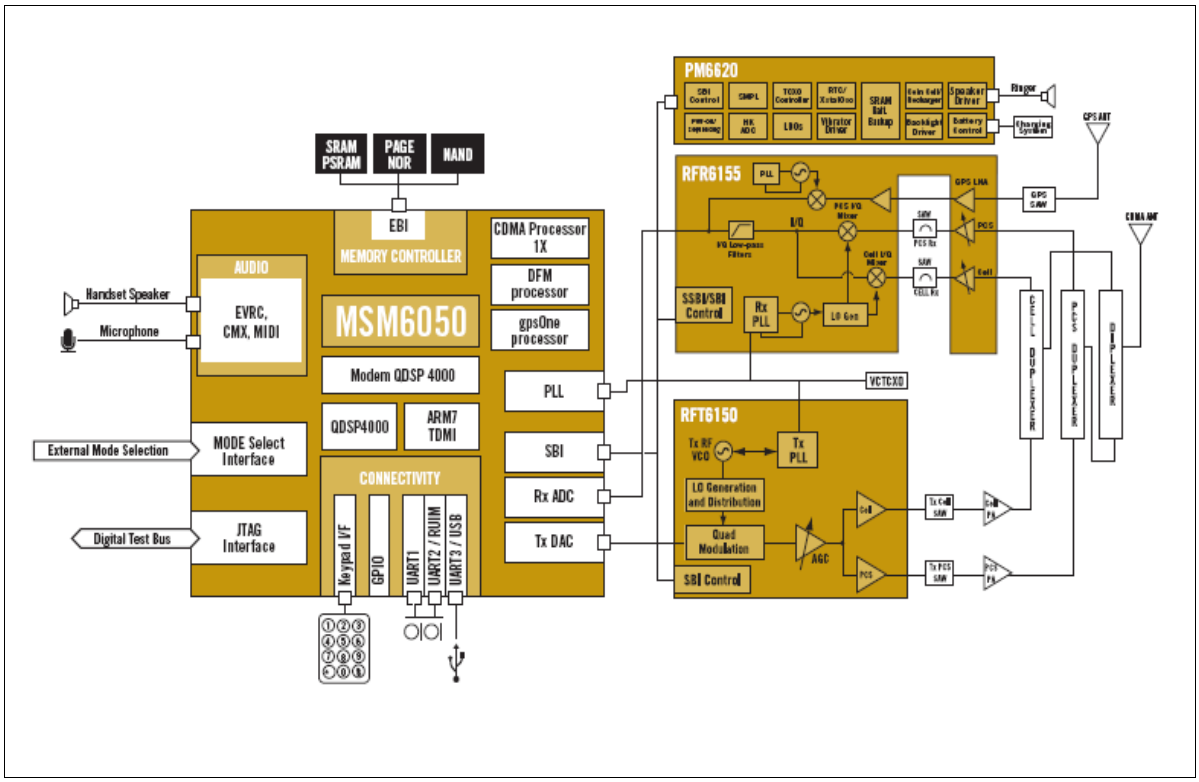
| | |
|---|---|
| 2. An interface according to claim 1<br><br>wherein said signals are transferred between said data transfer device and said transceiver in serial form. | The accused instrumentalities include each of the elements specified by Claim 1.<br><br>In addition, the HK ADC and the TX DAC included in the chip sets used in each accused instrumentality each use a serial bus to transfer data with the transceiver. Accordingly, data are transferred between the data transfer device and the transceiver in serial form in the accused instrumentalities.<br><br>  <br>Moreover, in instances where the data transfer device is implemented as a component attached to the Universal Serial Bus (USB), the data signals are necessarily being transferred serially, which is an inherent feature of the Universal Serial Bus, illustrated at the right. |
| 3. An interface according to claim 2<br><br>wherein said control means operates upon said transceiver to condition said transceiver to a transmit mode upon connection of said databus with said transmitting circuit. | The accused instrumentalities include each of the elements specified by Claim 2.<br><br>In addition, the control means in the form of a microprocessor or digital signal processor, such as the CDMA processor illustrated below, executing code functions to direct the transceiver to transmit when the control means and switch means operate to enable communication of data from the transmitting circuit to the transceiver over the data bus.<br><br>  |

| | |
|---|---|
| 4. An interface according to claim 2<br><br>wherein said control means is responsive to a change from an inactive to an active condition to connect said data bus to said transmitting circuit. | The accused instrumentalities include each of the elements specified by Claim 2.<br><br>In addition, the control means in the form of a microprocessor executing code functions to enable data transfer from the data bus to the transmitting circuit when the user desires to communicate information. Such activation is indicated by a change in logic state in one or more logic bits within the microprocessor executing the code. |
| 6. An interface according to claim 4<br><br>including amplifying means in said receiving circuit. | The accused instrumentalities include each of the elements specified by Claim 4.<br><br>The HK ADC, illustrated to the right, includes amplifying circuitry.<br><br>  |
| 7. An interface according to claim 6<br><br>wherein a buffer amplifier is included in said transmitting circuit to isolate said switch means and said transceiver. | The accused instrumentalities include each of the elements specified by Claim 6.<br><br>In addition, the TX DAC, illustrated to the right, includes buffer amplifier circuitry that effectively isolates the switch means and the transceiver.<br><br>  |

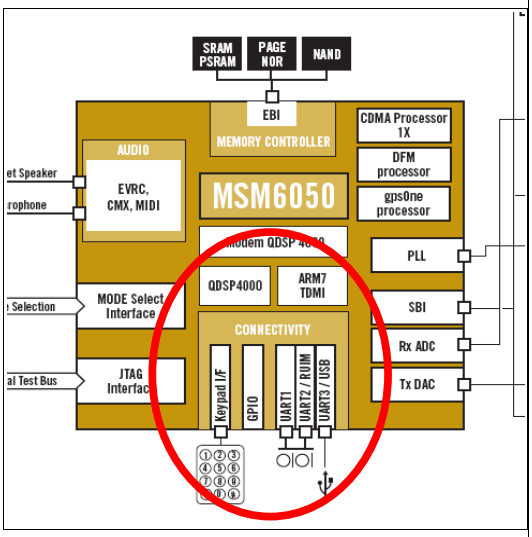
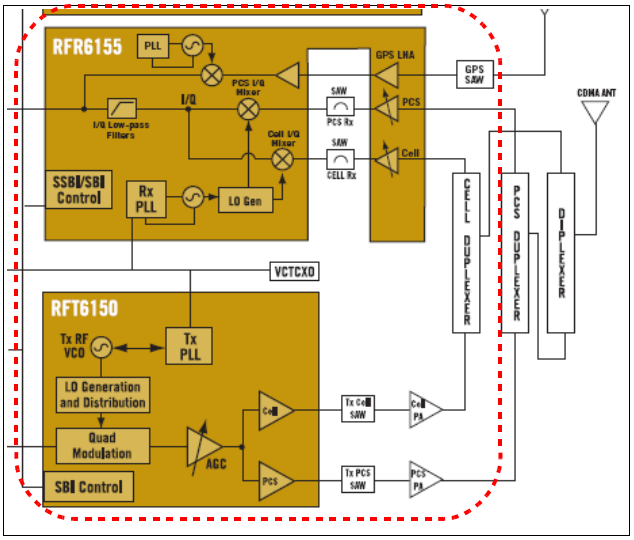
**MSM6050 Chipset**

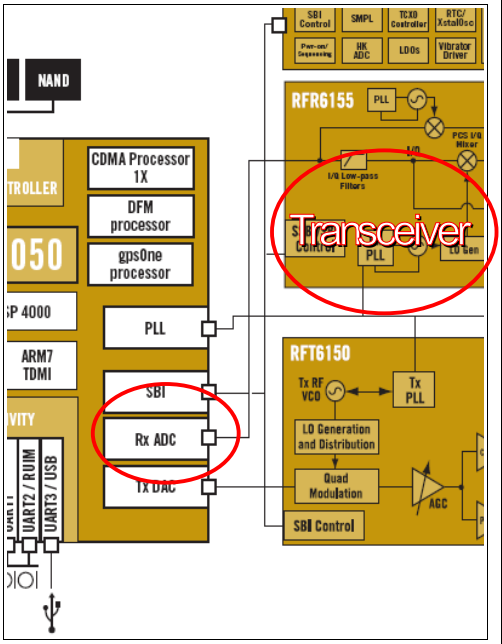
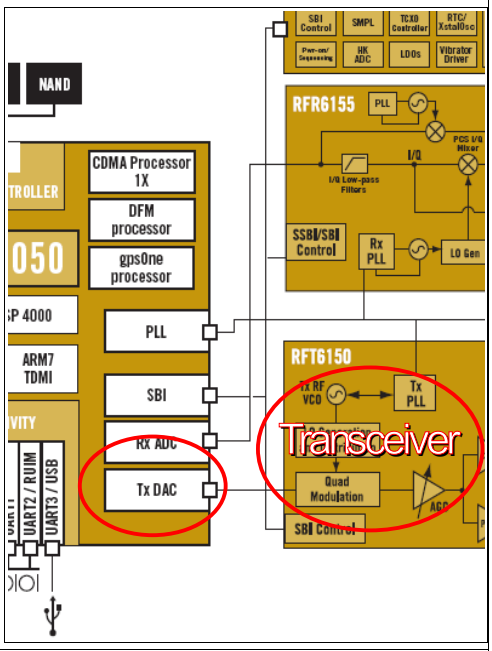
CCertain of Kyocera's wireless mobile devices have been manufactured and delivered incorporating the Qualcomm® MSM6050 chipset solution (pictured below). The MSM6050 chipset includes circuitry and componentry that causes the device to interface a data transfer device with a radio transceiver, as claimed in U.S. Patent 4,809,297.

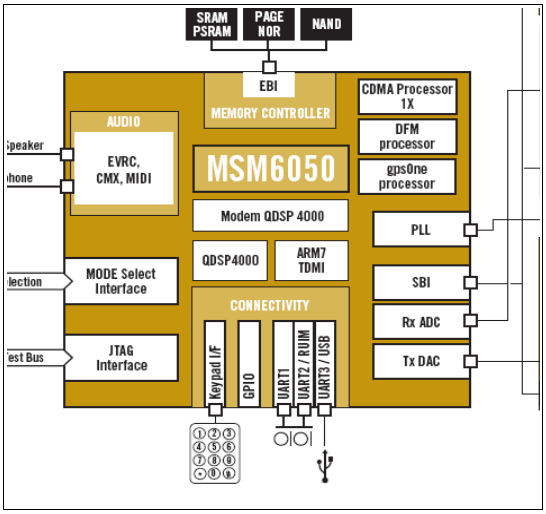
Plaintiff further alleges that other devices manufactured by Kyocera and other Defendants that incorporate the identified chipset also infringe in the same manner as detailed below. For the purpose of this Claim Chart, an "accused instrumentality" is any device of the Defendant that incorporates the MSM6050 chipset.

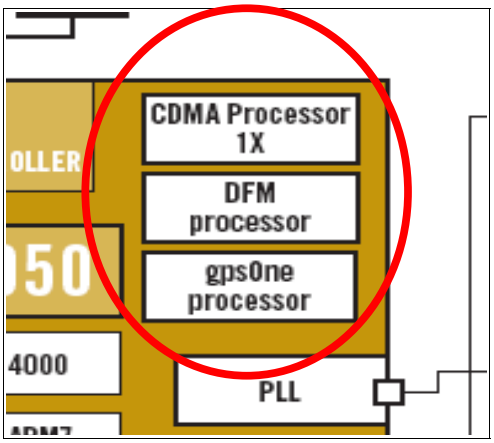


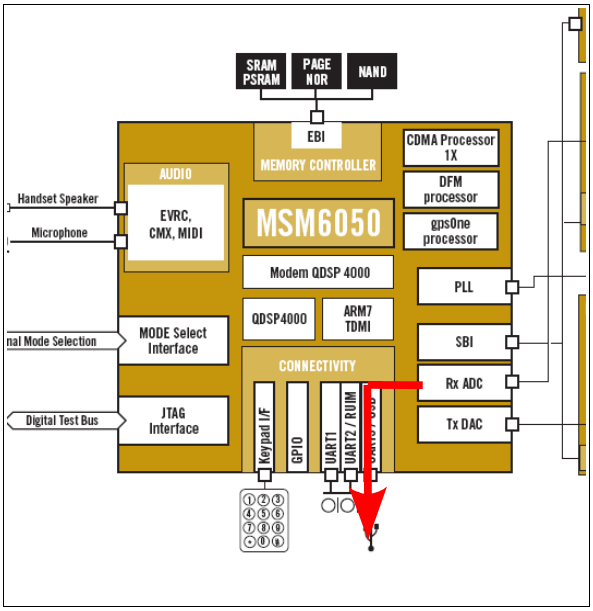
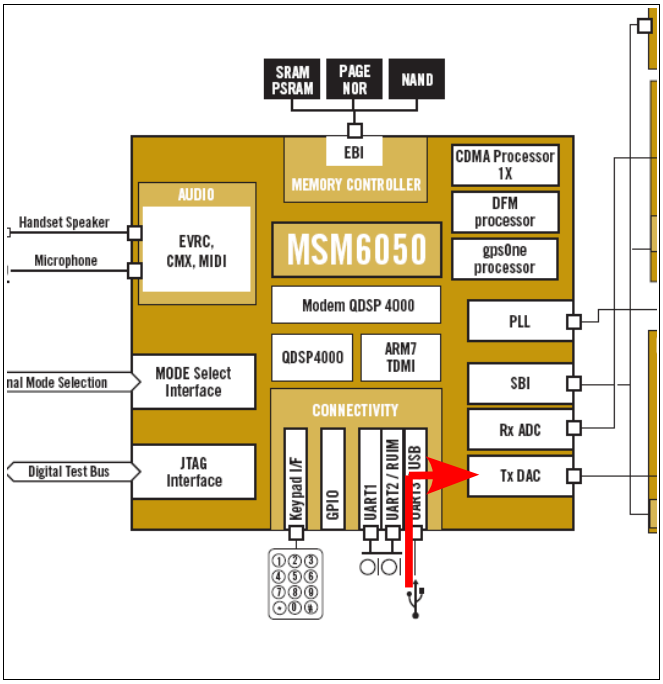
# CLAIM CHART

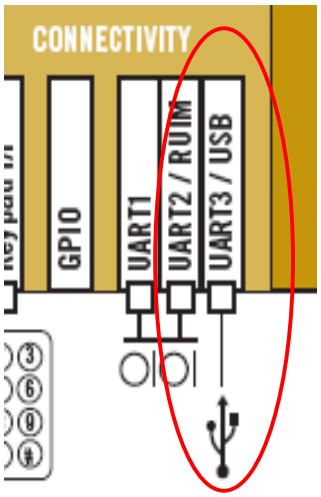
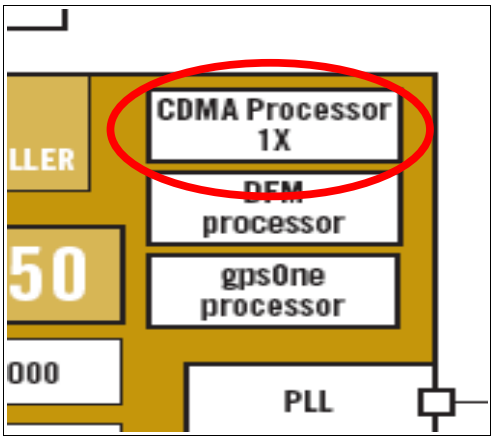
| | |
|---|---|
| 1. An interface to connect a data transfer device with a radio transceiver<br><br>*comprising:* | The accused device includes the chipset identified above, which is an interface to connect a data transfer device with a radio transceiver.<br><br>The accused device includes several components, any one or more of which constitute a data transfer device. In one example, the accused device includes a GPS receiver which is a data transfer device.<br><br>Other components coupled to the identified chipset may also constitute a "data transfer device", such as any one or more devices connected to the "Connectivity" portion of the identified chipset at right.<br><br>  <br><br>Data Transfer Devices |
| | The accused device further includes a radio transceiver as identified in the representative chipset diagram reproduced below. The components constituting the radio transceiver include the RFR6155, and RFT6150 components.<br><br>  <br><br>Transceiver Portion of MSM6050 Chipset |

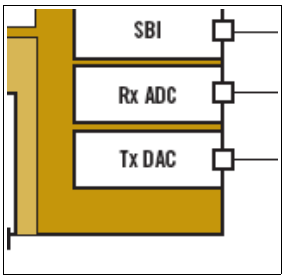
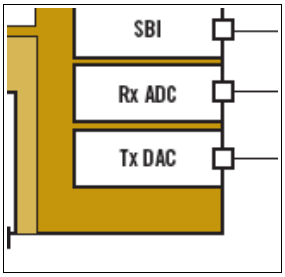
| | |
|---|---|
| a **receiving circuit** to receive a data signal in a given form from said **transceiver**, | The identified chipset embedded in the accused instrumentality includes a receiving circuit shown here as the "RX ADC" (receiving analog-to-digital converter).<br><br>The receiving circuit receives a data signal in a given form from the transceiver, identified here as component RFR6155.<br><br>  |
| a **transmitting circuit** to transmit a data signal in said given form to said **transceiver**, | The identified chipset embedded in the accused instrumentality includes a receiving circuit shown here as the "TX DAC" (transmitting digital-to-analog converter).<br><br>The transmitting circuit transmits a data signal in a given form to the transceiver, identified here as component RFT6150.<br><br>  |
| a data bus to transfer one of said data signals between said device and the respective circuit, | The identified chipset component includes a data bus within the MSM6050 chip that operates to transfer data between the data transfer device and the receiving circuit, and to transfer data between the data transfer device and the transmitting circuit.<br><br>In the accused instrumentalities, the data bus is at least partially contained within the integrated circuit forming the MSM6050 chip as a series of etched conductive paths or links between the functional blocks illustrated below in the chip set. The data bus also further includes or couples to any of the dual memory buses, |

| | |
|---|---|
| | the general-purpose interface bus, the address/data microprocessor bus and other internal buses<br>  |
| switch means to connect one of said circuits with said data bus | The accused instrumentalities include switch means that connect one of the receiving or transmitting circuits with the data bus. The identified chipset includes transistors and other logic gates for alternately coupling components of the chipset one to another for the purpose of isolating, blocking, routing and or conditioning of the data signals to connect the data bus with either of the receiving or transmitting circuits.<br><br>The switch means comprises various logic gates and transistors that are in electrical cooperation with each of the various sub-components of the identified chip set that perform the function of the switch means. These various logic gates and transistors function to effectively connect the transmitting circuit or the receiving circuit to the data bus. |
| and control means to control said switch means, | The accused instrumentalities include electronic circuitry operable to control the switch means, to connect one of the transmitting or receiving circuits with the data bus.<br><br>The control means is a microprocessor or digital signal processor (DSP) in the accused instrumentality executing code that provides logic for determining whether to connect one of the transmitting or receiving circuits with the data bus. The microprocessor is under control of the source code is a special purpose machine including various logic gates and transistors, such as AND gates, flip-flops and inverters, that perform the function of the control means. Such control means along with the switch means described above can be found in the CDMA processor, the gpsOne processor, and the |

| | |
|---|---|
| | DFM processor portions of the chipset illustrated below.<br>  <br>These processors control the switching means to effectively connect the transmitting circuit of the receiving circuit to the data bus, to control the operation of the bus connection according to the intended destination of the signal to of from the data transfer device, to follow the change in the operational mode, to disconnect the connection in the unwanted route, and to maintain the effective connection in the wanted route. |
| said control means being responsive to a signal from said data transfer device, | In the accused instrumentalities, the control means responds to a signal from any one or more of the data transfer devices. The signal comprises a change of state in one or more data bits that signals a change in the operational mode of the data transfer device and/or data ready to be transmitted or otherwise handled by the control means on behalf of the data transfer devices. |
| which is indicative of a change in the operational mode thereof | In the accused instrumentalities, the signal from the data transfer device consists of one or more bi-stable digital bits having states of logic “1” and logic “0” indicative of a change in operational mode respectively. A change from logic “0” to logic “1” or vice versa indicates a change in the operational mode of the data transfer device. |
| to disconnect said one circuit | In the accused instrumentalities, a change in logic state of the signal received from the data transfer device, results in the control means and switch means operatively terminating effective communication between one of the transmitting or receiving circuits over the data bus. |

| | |
|---|---|
| |  |
| and connect the other of said circuits to said data bus. | In the accused instrumentalities, a change in logic state of the signal received from the data transfer device, results in the control means and switch means operatively permitting effective communication between the other of the transmitting or receiving circuits over the data bus.<br>  |

| | |
|---|---|
| 2. An interface according to claim 1<br><br>wherein said signals are transferred between said data transfer device and said transceiver in serial form. | The accused instrumentalities include each of the elements specified by Claim 1.<br><br>In addition, the RX ADC and the TX DAC included in the chip sets used in each accused instrumentality each use a serial bus to transfer data with the transceiver. Accordingly, data are transferred between the data transfer device and the transceiver in serial form in the accused instrumentalities.<br><br>Moreover, in instances where the data transfer device is implemented as a component attached to the Universal Serial Bus (USB), the data signals are necessarily being transferred serially, which is an inherent feature of the Universal Serial Bus, illustrated at the right.<br><br>  |
| 3. An interface according to claim 2<br><br>wherein said control means operates upon said transceiver to condition said transceiver to a transmit mode upon connection of said databus with said transmitting circuit. | The accused instrumentalities include each of the elements specified by Claim 2.<br><br>In addition, the control means in the form of a microprocessor or digital signal processor, such as the CDMA processor illustrated below, executing code functions to direct the transceiver to transmit when the control means and switch means operate to enable communication of data from the transmitting circuit to the transceiver over the data bus.<br><br>  |

| | |
|---|---|
| 4. An interface according to claim 2<br><br>wherein said control means is responsive to a change from an inactive to an active condition to connect said data bus to said transmitting circuit. | The accused instrumentalities include each of the elements specified by Claim 2.<br><br>In addition, the control means in the form of a microprocessor executing code functions to enable data transfer from the data bus to the transmitting circuit when the user desires to communicate information. Such activation is indicated by a change in logic state in one or more logic bits within the microprocessor executing the code. |
| 6. An interface according to claim 4<br><br>including amplifying means in said receiving circuit. | The accused instrumentalities include each of the elements specified by Claim 4.<br><br>The RX ADC, illustrated to the right, includes amplifying circuitry.  |
| 7. An interface according to claim 6<br><br>wherein a buffer amplifier is included in said transmitting circuit to isolate said switch means and said transceiver. | The accused instrumentalities include each of the elements specified by Claim 6.<br><br>In addition, the TX DAC, illustrated to the right, includes buffer amplifier circuitry that effectively isolates the switch means and the transceiver.  |